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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,306	04/01/2004	Katsuya Shinohara	56937-111	8591

7590 01/26/2007

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EXAMINER	
PATEL, SHAMBHAVI K	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,306	SHINOHARA, KATSUYA	
	Examiner	Art Unit	
	Shambhavi Patel	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/24/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6 and 8 are pending. Claim 7 has been cancelled.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 24 October 2006 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Arguments

3. Applicant's arguments filed 24 October 2006 have been fully considered but they are not persuasive.

i. Applicant submits that Ghosh fails to disclose "a plurality of simulator models each including a functional model for a CPU constituting a system to be simulated." Applicant is directed to the **last paragraph in "Introduction"**, which states "In section 3 we present **different CPU models**", **section 3.1.1 2nd paragraph,** which states (emphasis added) "This allows the user to **swap one processor model for another** easily." Ghosh discloses multiple simulation models (see for example, section 3.1.1 which discloses different BFMs), each containing a CPU.

ii. Applicant submits that because Ghosh discloses "the interface methods have the same prototype for all BFMs", he does not disclose or suggest "plural types of interfaces included in the simulator models and enabling plural types of simulators for various uses." The Examiner notes that the portion of Ghosh cited by the Applicant fully reads (emphasis added): "In the SYSTEMC environment, the programming interface to BFMs is more or less fixed, i.e. the interface methods have the same prototype for all BFMs,

though some BFMs may support methods that are not supported in others." Thus, while the prototypes for the methods are the same, different interfaces contain different methods, and thus the Examiner maintains that Ghosh discloses plural types of interfaces. Applicant is directed to **section 3.2 1st paragraph**, which states "Different types of ISS can be developed for different purposes."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claim 1-6 and 8 are rejected under 35 U.S.C. 102(b)** as being clearly anticipated by **Ghosh et al. ('Methodology for Hardware/Software Co-Verification in C/C++)**, herein referred to as Ghosh.

Regarding claim 1:

Ghosh discloses a simulator apparatus comprising:

a. a plurality of simulator models each including a functional model for CPU constituting a system to be simulated **('Introduction' last paragraph; section 3.1 'Bus Functional Model'; section 3.1.1. 'Design of the BFM' 2nd paragraph)**

b. a simulator model including a functional model for hardware to be connected to buses linked to the corresponding CPU **(section 2 'Design Flow' paragraph 2; section 3.1.2 'Memory-mapped I/O' 1st paragraph)**

c. plural types of interfaces included in the simulator models and enabling plural types of simulators for various uses to access to the functional models **(section 3.1.2 'Memory Mapped I/O' paragraphs 3-4; section 3.2 'Instruction set simulator' 1st paragraph)**

d. a simulator controlling device for selecting any of the plural types of the interfaces and accessing the respective functional models via the selected interfaces **(section 3.1.2 'Memory Mapped I/O' paragraphs 3-4)**

Regarding claim 2:

Ghosh discloses a simulator apparatus as claimed in claim 1, wherein the interfaces for the respective functional models comprise an interface usable in a simulator for verifying software **('Introduction' paragraph 6; section 3.2 'Instruction Set Simulator')**.

Regarding claim 3:

Ghosh discloses a simulator apparatus as claimed in claim 1, wherein the interfaces for the respective functional models comprise an interface usable in a simulator for verifying hardware **('Introduction' paragraph 6; section 3.2 'Instruction Set Simulator')**.

Regarding claim 4:

Ghosh discloses a simulator apparatus as claimed in claim 1, wherein the interfaces for the respective functional models comprise an interface usable in a simulator for verifying a system **('Introduction' paragraph 6; section 3.2 'Instruction Set Simulator')**.

Regarding claim 5:

Ghosh discloses a simulator apparatus as claimed in claim 1, wherein the interfaces for the respective functional models comprise an interface usable in debugging **(section 3.1.6 'Performance Estimation Functions' paragraph 2)**

Regarding claim 6:

Ghosh discloses a simulator apparatus as claimed in claim 1, wherein an interface to perform precise simulation for the system at clock level **(section 3.1.1 'Design of the BFM' 1st paragraph)**. As per the specification, this limitation is interpreted to mean that the output from the simulation correspond to the outputs of the pins. The prior art discloses that the ports in the modules correspond to the hardware pins, and thus the output of the ports is tied to the output of the pins.

Regarding claim 7:

Cancelled

Regarding claim 8:

Ghosh discloses a simulator apparatus as claimed in claim 1, wherein the interfaces for the respective functional models comprise an interface for extension usable in performance analysis **(section 3.1.6 'Performance Estimation Functions' paragraph 2)**.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is (571) 272-5877. The examiner can normally be reached on Monday-Friday, 8:00 am – 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SKP

Shambhavi Patel
Examiner
Art Unit 2128

KAMINI SHAH
SUPERVISORY PATENT EXAMINER